**Digital Electronics and Computer Architecture Laboratory**

**Assignment Number: 05**

**PROBLEM STATEMENT:**

Design and Implement 3 bit Synchronous UP Counterusing JK- Flip flop

**Objectives:**

* To understand the operation of Synchronous counter
* To design and implement 3-Bit Synchronous UP counter using JK- Flip flop

**IC’s Used:**

|  |  |
| --- | --- |
| **IC Number** | **IC Name** |
| 74LS76 | Dual MS JK Flip Flop |
| 74LS08 | Quad 2-Input AND Gate |

**PLATFORM USED:** [**https://www.deldsim.com/simulator/**](https://www.deldsim.com/simulator/)

**Theory:**

1. Definition of Synchronous counter
2. Advantages of Synchronous counter
3. Application of Synchronous counter

**Procedure:**

1. Design Sequential circuit logic circuit as per given problem statement.
2. Connect the IC 74LS76 and other basic logic gate ICs as per diagram.
3. Give VCC supply and ground connection to each IC.
4. Give clock to all JK FFs.
5. Observe the output and verify the truth table.
6. Switch off the power supply of trainer kit.

**Draw Circuit Diagram 3-Bit DOWN Synchronous.**

**Conclusion:**

**Post Lab Questions:**

1. Why a synchronous counter operate at a higher frequency than a ripple counter?
2. A 5-bit synchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is \_\_\_\_\_\_\_\_\_\_\_\_?